Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-5. (Cancelled).

6. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film ~~so that crystal growths proceed in crystal growth directions parallel to the insulating surface~~ from the first metal element added region and the second metal element added region ~~thereby~~ to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a functional array of semiconductor islands, using [[only]] the first crystalline portion while the second crystalline portion is not used to form ~~the~~ any crystalline semiconductor island of the functional array of semiconductor islands,

wherein the second crystalline portion is located between the crystalline semiconductor island and the second metal element added region,

wherein the first metal element added region is away from the second metal element added region~~,~~

~~wherein carriers move in the crystalline semiconductor island in a carrier moving direction identical with the crystal growth direction,~~

~~wherein the second metal element added region is located apart from the crystalline semiconductor island by a distance, and~~

~~wherein the first metal element added region has a length extending longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region~~.

7. (Previously Presented) The method according to claim 6,

wherein lengths of the first metal element added region and the second element added region are set to 50% or more of a crystal growth distance.

8. (Previously Presented) The method according to claim 6,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

9. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

~~selectively~~ providing a metal element being capable of promoting crystallization of the amorphous semiconductor film ~~into at least a first region and a second region of the amorphous semiconductor film~~ to form a first metal element added region and a second metal element added region~~, respectively~~;

crystallizing the amorphous semiconductor film ~~so that crystal growths proceed in parallel to the insulating surface~~ from ~~each of~~ the first metal element added region and the second metal element added region to form a first crystalline ~~semiconductor region~~ portion and a second crystalline ~~semiconductor region~~portion, respectively, in a crystalline semiconductor film; and

~~forming at least one active region of the semiconductor device in the first~~ patterning the crystalline semiconductor film to form at least one crystalline semiconductor ~~region~~ island of a functional array of semiconductor islands, using the first crystalline portion while the second crystalline ~~semiconductor region~~ portion is not used to form ~~an active region of the~~

~~semiconductor device~~ any crystalline semiconductor island of the functional array of semiconductor islands,

wherein the second metal element added region is located at a peripheral edge of the group of active elements, and

wherein the first metal element added region is away from the second metal element added region.

10. (Previously Presented) The method according to claim 9,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

11. (Previously Presented) The method according to claim 9,

wherein the metal element is provided by an ion implanting method.

12. (Previously Presented) The method according to claim 9,

wherein the metal element is provided by coating a solvent comprising the metal element.

13. (Cancelled).

14. (Previously Presented) The method according to claim 9,

wherein the amorphous semiconductor film comprises silicon.

15. (Previously Presented) The method according to claim 9,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

16. (Previously Presented) The method according to claim 9,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

17. (Cancelled).

18. (Previously Presented) The method according to claim 6,

wherein the amorphous semiconductor film comprises silicon.

19. (Cancelled).

20. (Previously Presented) The method according to claim 6,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

21. (Previously Presented) The method according to claim 6,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

22. (Cancelled).

23. (Previously Presented) The method according to claim 9,

wherein crystal growth state is controlled by the second metal element added region.

24. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to form a ~~selected~~ first metal element added region ~~of the amorphous semiconductor film~~and a second metal element added region;

crystallizing the amorphous semiconductor film from the first metal element added region and the second metal element added region to form a first crystalline ~~semiconductor film so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region~~portion and a second crystalline portion, respectively, in a crystalline semiconductor film; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a functional array of semiconductor islands, using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the functional array of semiconductor islands,

wherein the ~~metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region~~ second crystalline portion extends along an entire length of the second metal element added region, and

wherein the first metal element added region is away from the second metal element added region.

25. (Previously Presented) The method according to claim 24,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

26. (Previously Presented) The method according to claim 24,

wherein the metal element is provided by an ion implanting method.

27. (Previously Presented) The method according to claim 24,

wherein the metal element is provided by coating a solvent comprising the metal element.

28. (Previously Presented) The method according to claim 24,

wherein the amorphous semiconductor film comprises silicon.

29. (Previously Presented) The method according to claim 24,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

30. (Previously Presented) The method according to claim 24,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

31. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to ~~at least two disconnected selected regions of the amorphous~~

~~semiconductor film~~ form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film from the first metal element added region and the second metal element added region to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film so that crystal growths proceed in directions parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a group of active elements using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the group of active elements,

wherein the second crystalline portion is located between the crystalline semiconductor island and the second metal element added region, and

wherein ~~a portion of the crystalline semiconductor film formed by using one~~ the first metal element added region is ~~not used to form crystalline semiconductor islands~~away from the second metal element added region.

32. (Previously Presented) The method according to claim 31,

wherein lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

33. (Previously Presented) The method according to claim 31,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

34. (Previously Presented) The method according to claim 31,

wherein the metal element is provided by an ion implanting method.

35. (Previously Presented) The method according to claim 31,

wherein the metal element is provided by coating a solvent comprising the metal element.

36. (Previously Presented) The method according to claim 31,

wherein the amorphous semiconductor film comprises silicon.

37. (Previously Presented) The method according to claim 31,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

38. (Previously Presented) The method according to claim 31,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

39. (Previously Presented) The method according to claim 31,

wherein crystal growth state is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

40. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to ~~at least two disconnected selected regions of the amorphous~~

~~semiconductor film~~form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film from the first metal element added region and the second metal element added region to form a first crystalline ~~semiconductor film so that crystal growths proceed in directions parallel to the insulating surface from metal element added regions~~portion and a second crystalline portion, respectively, in a crystalline semiconductor film; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a group of active elements using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the group of active elements,

wherein ~~at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of a metal element added region~~the second crystalline portion is located at a peripheral edge of the group of active elements, and

wherein ~~a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands~~the first metal element added region is away from the second metal element added region.

41. (Previously Presented) The method according to claim 40,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

42. (Previously Presented) The method according to claim 40,

wherein the metal element is provided by an ion implanting method.

43. (Previously Presented) The method according to claim 40,

wherein the metal element is provided by coating a solvent comprising the metal element.

44. (Previously Presented) The method according to claim 40,

wherein the amorphous semiconductor film comprises silicon.

45. (Previously Presented) The method according to claim 40,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

46. (Previously Presented) The method according to claim 40,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

47. (Previously Presented) The method according to claim 40,

wherein crystal growth state is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

48. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to ~~a selected region of the amorphous semiconductor film~~form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film ~~so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region~~; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a group of active elements using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the group of active elements,

wherein the ~~metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region~~ second crystalline portion extends along an entire length of the second metal element added region, and

wherein the ~~crystalline semiconductor island constitutes a TFT of an inverter circuit~~ first metal added region is away from the second metal element added region.

49. (Previously Presented) The method according to claim 48,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

50. (Previously Presented) The method according to claim 48,

wherein the metal element is provided by an ion implanting method.

51. (Previously Presented) The method according to claim 48,

wherein the metal element is provided by coating a solvent comprising the metal element.

52. (Previously Presented) The method according to claim 48,

wherein the amorphous semiconductor film comprises silicon.

53. (Previously Presented) The method according to claim 48,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

54. (Previously Presented) The method according to claim 48,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

55. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to ~~at least two disconnected selected regions of the amorphous semiconductor film~~ form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film from the first metal element added region and the second metal element added region to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film ~~so that crystal growths proceed in directions parallel to the insulating surface from metal element added regions~~; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a functional array of crystalline semiconductor islands using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the functional array of semiconductor islands,

wherein the second crystalline portion is located between the crystalline semiconductor island and the second metal element added region,

wherein ~~a portion of the crystalline semiconductor film formed by using one~~ the first metal element added region is ~~not used to form crystalline semiconductor islands~~away from the second metal element added region, and

wherein the crystalline semiconductor island constitutes a TFT of an inverter circuit.

56. (Previously Presented) The method according to claim 55,

wherein lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

57. (Previously Presented) The method according to claim 55,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

58. (Previously Presented) The method according to claim 55,

wherein the metal element is provided by an ion implanting method.

59. (Previously Presented) The method according to claim 55,

wherein the metal element is provided by coating a solvent comprising the metal element.

60. (Previously Presented) The method according to claim 55,

wherein the amorphous semiconductor film comprises silicon.

61. (Previously Presented) The method according to claim 55,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

62. (Previously Presented) The method according to claim 55,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

63. (Previously Presented) The method according to claim 55,

wherein crystal growth state is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

64. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to ~~at least two disconnected selected regions of the amorphous semiconductor film~~ form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film from the first metal element added region and the second metal element added region to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film ~~so that crystal growths proceed in directions parallel to the insulating surface from metal element added regions~~; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island of a group of active elements using the first crystalline portion while the second crystalline portion is not used to form any crystalline semiconductor island of the group of active elements,

wherein ~~at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of a metal element added region~~the second crystalline portion is located between the crystalline semiconductor island and the second metal element added region, ~~and~~

wherein ~~a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands~~the first metal element added region is away from the second metal element added region, and

wherein the crystalline semiconductor island constitutes a TFT of an inverter circuit.

65. (Previously Presented) The method according to claim 64,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

66. (Previously Presented) The method according to claim 64,

wherein the metal element is provided by an ion implanting method.

67. (Previously Presented) The method according to claim 64,

wherein the metal element is provided by coating a solvent comprising the metal element.

68. (Previously Presented) The method according to claim 64,

wherein the amorphous semiconductor film comprises silicon.

69. (Previously Presented) The method according to claim 64,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

70. (Previously Presented) The method according to claim 64,

wherein the inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

71. (Previously Presented) The method according to claim 64,

wherein crystal growth state is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

72. (New) The method of claim 6,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

73. (New) The method of claim 9,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

74. (New) The method of claim 24,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

75. (New) The method of claim 31,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

76. (New) The method of claim 40,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

77. (New) The method of claim 48,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

78. (New) The method of claim 55,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

79. (New) The method of claim 64,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.